# PATENT ABSTRACTS OF JAPAN

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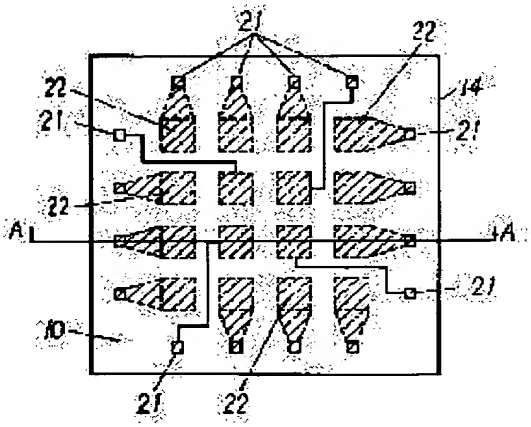
## (54) SUPPORTING SUBSTRATE OF SEMICONDUCTOR ELEMENT AND CIRCUIT DEVICE USING THE SAME

(57)Abstract:

PURPOSE: To diminish the defects in circuit device due to the stress concentration by improving the arrangement of conventional bump electrodes in relation to the title supporting substrate of semiconductor elements connected by the bump electrodes between circuit substrates and semiconductor elements when the semiconductor elements are flip chip-packaged.

CONSTITUTION: Electrode terminals 21 are arranged on the positions opposite to the electrode terminals arranged along the outer peripheries of semiconductor elements on the surface of a supporting substrate 14. The other element terminals 22 in continuity to the electrode terminals 21 on the surface are arranged on the rear surface of the supporting substrate 14 taking chessboard cross shape. These electrode terminals 21, 22 are connected to the semiconductor elements and circuit substrates by bump electrodes. Through these procedures, the stress imposed by the difference in the thermal expansion coefficients of the semiconductor elements and the circuit substrates can be dispersed in the bump electrodes arranged taking chessboard cross shape.

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CLAIMS

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[Claim(s)]
[Claim 1] It is arranged between the circuit board and the semiconductor device in which the electrode terminal was prepared along with the periphery section. In a front face, the electrode terminal of said semiconductor device, and the 1st electrode terminal connected through a projection electrode to the electrode terminal of said semiconductor device, and the location which counters It is the substrate which has the electrode terminal which flowed with said 1st electrode terminal in the rear face, and was prepared in said circuit board through other projection electrodes, and the 2nd electrode terminal connected. The support substrate of the semiconductor device characterized by having arranged said 2nd electrode terminal also in the location inside said 1st electrode terminal so that one of the 2nd electrode terminal arranged at the rear face of said substrate at least may not counter with said 1st electrode terminal.
[Claim 2] The support substrate of the semiconductor device according to claim 1 characterized by forming the 1st electrode terminal and 2nd electrode terminal in a respectively different conductor layer.
[Claim 3] The support substrate of the semiconductor device according to claim 1 characterized by forming in the longitudinal direction of said base material in succession with the electrode for a trial connected to the 1st electrode terminal on the base material of the shape of a tape which has flexibility.
[Claim 4] The 1st electrode terminal is arranged in said electrode terminal of the semiconductor device by which the electrode terminal was prepared in the front face along with the periphery section, and the location which counters. As said 1st electrode terminal and the 2nd flowing electrode terminal arranged in the rear face and not countered in one of said the 2nd electrode terminal with said 1st electrode terminal at least The support substrate which has arranged said 2nd electrode terminal also in the location inside said 1st electrode terminal It is made to intervene between a semiconductor device, said 2nd electrode terminal, and the circuit board that prepared the electrode terminal in the location which counters. Between said 1st electrode terminal and electrode terminals of said semiconductor device, The circuit apparatus which used the support substrate of the semiconductor device characterized by coming to connect between said 2nd electrode terminal and electrode terminals of the circuit board through a projection electrode, respectively.
[Claim 5] The 1st electrode terminal is arranged in said electrode terminal of the semiconductor device by which the electrode terminal was prepared in the front face along with the periphery section, and the location which counters. As said 1st electrode terminal and the 2nd flowing electrode terminal arranged in the rear face and not countered in one of said the 2nd electrode terminal with said 1st electrode terminal at least While making the support substrate which has arranged said 2nd electrode terminal also in the location inside said 1st electrode terminal intervene between the circuit boards which prepared the semiconductor device and the electrode terminal The 2nd electrode terminal of a support substrate or the electrode terminal of said circuit board, and 2nd at least one or more support substrates that prepared the electrode terminal in the location which counters are made to intervene between said circuit boards and said support substrates. The circuit apparatus which used the support substrate of the semiconductor device characterized by coming to connect between the electrode terminals which counter, respectively through a projection electrode.

[Translation done.]



DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention distributes the stress produced according to the difference of the coefficient of thermal expansion of the semiconductor device and substrate which were mounted by the flip chip method, and relates to the circuit apparatus which used the support substrate of the semiconductor device for raising dependability, and it.
[0002]
[Description of the Prior Art] In recent years, development of the device using many semiconductor devices is promoted. In order to set to the semi-conductor mounting approach, to miniaturize a device more and to have advanced features, examination of the higher-density mounting approach is performed and it is shifting to the QFP mold which is a surface mounting mold from the DIL mold package which is the conventional inserting type at the WAYA bonding method and flip chip (it abbreviates to FC method below) which do not carry out the resin mold of the semiconductor device further and which are a bare chip mounting method.
[0003] The conventional FC method is explained using drawing 8 below. In drawing, as for the electrode terminal (it is called a pad below) with which 11 was formed in the semiconductor device (it is called a chip below), and 12 was formed on the chip, and 13, a projection electrode (it is called a bump below) and 15 are the circuit boards, and 16 is the pad formed on the circuit board 15. Such a FC method has an occupancy area equivalent to the size of a chip 11 to the circuit board 15 of a chip 11, and can obtain a very high-density device. Moreover, the wire length between a chip 11 and the circuit board 15 becomes extremely short compared with other mounting methods, and degradation of a RF property and the delay of a signal by the eddy current are also improved.
[0004] However, with the above-mentioned configuration, since the coefficient of thermal expansion of the circuit board 15 is large compared with a chip 11, it is easy to fracture a bump 13 with the stress produced in the thermo-cycle trial from a pad 12 and the circuit board 15. this -- stress -- receiving -- dependability -- raising -- a sake -- a bump -- height -- high -- carrying out -- if -- a thermo cycle -- a sex -- improving -- ** -- saying -- a report -- it is -- although -- a bump -- an ingredient -- ****** -- solder -- having used -- a case -- a bump -- 13 -- high -- carrying out -- a sake -- **** -- a pad -- 12 -- size -- large -- it must carry out -- a result -- a chip -- 11 -- the very thing -- large -- it must carry out -- high density assembly -- from -- having been widely different -- mounting -- a gestalt -- becoming .
[0005] Then, the support substrate 14 made of resin is made to intervene between a chip 11 and the circuit board 15, as shown in drawing 9 a. Between each is connected by Bumps 13a, 13b, and 13c.

Thermo-cycle nature will be raised without changing the magnitude of a chip 11. What is carried out is proposed (). [ "VLSI ] CHIP INTERCONNECTION TECHNOLOGY USING STACKED SOLDER BUNPS" IMC 1998 Proceedings, Tokyo, and May25- 27 and 1988. As this support substrate 14 is shown in the top view of this drawing b, the pad 17 is formed in the periphery section so that the pad 12 of a chip 11 and the pad 16 of the circuit board 15 may be countered. As shown in the expanded sectional view of the support substrate 14 of this drawing c, this pad 17 is formed on the bore 32 formed in the film 33 made of resin used as the base material of the support substrate 14, and is having structure which covered the both sides of the metal layer 31 of Ti with copper 30.

[0006]

[Problem(s) to be Solved by the Invention] However, also in FC method which forms the support substrate 14 as mentioned above, since the pad 17 was formed only in the location corresponding to the electrode terminal prepared in the periphery section of a chip 11, the stress produced in a thermo-cycle trial according to the difference of the coefficient of thermal expansion of a chip 11 and the circuit board 15 concentrated on the bump of the periphery section, and it had the problem that dependability was inferior still more.

[0007]

[Means for Solving the Problem] In order to solve the above-mentioned technical problem, the support substrate of the semiconductor device of this invention It is arranged between the circuit board and the semiconductor device in which the electrode terminal was prepared along with the periphery section. In a front face, the electrode terminal of said semiconductor device, and the 1st electrode terminal connected through a projection electrode to the electrode terminal of said semiconductor device, and the location which counters It is the support substrate which has the electrode terminal which flowed with said 1st electrode terminal in the rear face, and was prepared in said circuit board through other projection electrodes, and the 2nd electrode terminal connected. Said 2nd electrode terminal is arranged also in the location inside said 1st electrode terminal so that one of the 2nd electrode terminal arranged at the rear face of said substrate at least may not counter with said 1st electrode terminal.

[0008]

[Function] With this configuration, the stress produced in a chip or a wiring substrate according to the difference of a coefficient of thermal expansion is distributed by the bump who distributed all over the chip occupied area of a support substrate, and has been stationed. For this reason, compared with what has stationed the bump in the periphery section, the stress produced by each bump becomes small, and that dependability improves by leaps and bounds in a thermo-cycle trial.

[0009]

[Example] The example of this invention is explained below, referring to a drawing. Drawing 1 shows the top view of the support substrate of the semi-conductor in the 1st example of this invention. In drawing, the support substrate 14 forms the pad 21 to which a bump is connected so that the pad of a chip may be countered at the periphery section of the front face of a base material 10, and it comes to form the pad 22 for connecting with the circuit board 15 through a bump in the rear face of a base material 10 in a grid pattern. Drawing 3 shows the A-A cross section of drawing 1 , and the pad 21 and the pad 22 have flowed through it electrically inside the support substrate 14, it prepares beforehand the bore for forming the conductive layer 24 which forms each pad 21 and 22 in a base material 10, and he is trying to form the support substrate 14 there by lamination etc.

[0010] Moreover, the mounting approach connects the pad 21 of the chip 11 with which bump 13a was formed first, and the support substrate 14, as shown in drawing 2 , and after it subsequently forms bump 13b in the pad 22 of the rear face of the support substrate 14 in a grid pattern, respectively, it connects it with the circuit board 15. In addition, the module which forms the bump ingredient in circuit board top 15 beforehand besides the mounting approach described previously, and connected the chip 11 to the support substrate 14 may be installed, a module and the circuit board 15 may be connected with heating, Bumps 13a and 13b are further formed on the support substrate 14, and the chip and support substrate

14 and the circuit board 15 may be connected by package by approaches, such as heating after alignment.

[0011] Since bump 13b will be arranged in a grid pattern, the stress produced between a chip 11 and the circuit board 15 can be distributed and spacing of a chip 11 and the circuit board 14 can be extended, the effect of stress decreases [ if such a support substrate 14 is used, ] further. Thus, compared with what formed the bump only in the periphery section between a support substrate and the circuit board, fracture of the bump by stress etc. decreases and the reliable FC mounting approach is acquired.

[0012] Moreover, between the support substrate 14 and the circuit board 15, the pad 22 of the support substrate 14 and the pad of the circuit board 15 as shown in drawing 4 , and the 2nd support substrate 19 in which the pad 33 was formed in the location which counters may be made to be able to intervene, spacing of a chip 11 and the circuit board 15 can be further extended using a majority of these support substrates, and dependability can also be raised further.

[0013] Now, according to the above-mentioned support substrate 14, the pad of a pad 22 and they, and the circuit board 15 that counters can be formed more greatly than the conventional thing by arranging pad 13b at the whole rear face of the support substrate 14. Therefore, positioning with the support substrate 14 at the time of mounting and the circuit board 15 can be made easier than the conventional thing.

[0014] Drawing 5 shows the 2nd example of this invention. in the 1st above-mentioned example, since said conductive layer 24 comes out further and is formed, it cannot arrange a pad 22 just under a pad 21, and cannot necessarily utilize the rear face of the support substrate 14 effectively. What is necessary is to form the conductive layer of a pad 21, and the conductive layer of a pad 22 in the support substrate 14 two-layer, and just to make it the configuration which makes it flow through between vertical conductive layers, as shown in this drawing c of the B-B cross section in order to arrange a pad 22 also just under a pad 21, as shown in drawing 5 a. What is necessary is just to carry out to connection between vertical conductive layers by known approach like plating.

[0015] Since spacing between each pad can moreover also make a pad 22 large greatly, moreover, the support substrate 14 formed as mentioned above can also open and arrange greatly the pad 16 of Bengbu 13b or the circuit board 15 for spacing, as shown in the sectional view of the circuit apparatus of this drawing b. For this reason, when the alignment of the circuit board 15 and the support substrate 14 becomes easy and uses the ceramic substrate using a green sheet method as the circuit board especially, it can cover completely that the location of the pad of the circuit board 15 by green sheet contraction dispersion at the time of baking varies, and it becomes possible to suppress extremely the fall of the yield by the alignment at the time of mounting.

[0016] Moreover, the support substrate 14 in this example can divert the test equipment and the facility which are used for mounting with the usual tape career method, and can raise continuation productivity. That is, if the support substrate 14 is formed succeeding the film 5 of the shape of a tape which has flexibility as shown in drawing 6 , as shown in drawing 7 , the mass production called reel tow reel will be attained. In drawing 6 , 2 is an electrode for a trial which flows in a pad 21, and a broken line 3 is the dimension of a chip 11. At the time of mounting of a chip 11, after supplying the film 5 with which the constant width which formed the sprocket hole 4 continued from the supply reel 6 to a take up reel 7 and connecting a chip 11 to a pad 21 through bump 13a in a work area W, the electrode 2 for a trial performs the trial after connection of a chip 11. Only an excellent article is pierced by said chip appearance 3 after this process, and it connects with the circuit board 15.

[0017] Thus, by forming the support substrate 14 and the electrode 2 for a trial in the shape of a tape, after connecting a chip 11 on the support substrate 14, a trial becomes possible as a module, and in-line inspection can be easily conducted now. Thereby, the mounting yield to the circuit board 15 can be raised by leaps and bounds, and the good mounting approach of workability is acquired. Moreover, the electrode 2 for a trial may be formed in the rear face or both sides of a film 5.

[0018] In addition, in the above example, although the pad has been arranged in a grid pattern at the

rear face of a support substrate, the whole rear face of a support substrate is used effectively, and as long as it distributes the stress generated in a bump, you may make it other arrays.

[0019]

[Effect of the Invention] Since the support substrate of the semiconductor device of this invention distributed all over the support substrate and has arranged the pad for connecting with the circuit board through a bump as mentioned above, the deformation and stress which are produced according to the difference of a coefficient of thermal expansion with the circuit board become remarkably small. For this reason, a circuit apparatus with the high dependability in a thermo cycle can be offered. Moreover, the magnitude of these pads is also large compared with the conventional thing, and positioning at the time of mounting can be performed easily, without being influenced by dispersion in the electrode location of the circuit board since spacing can moreover be opened and formed. Furthermore, a mass production by the reel tow reel can also raise the mounting yield by conducting the performance test of a chip, where it was possible and a chip is put on a support substrate.

[0020] Moreover, if the electrode terminal of a support substrate or the electrode terminal of the circuit board, and 2nd at least one or more support substrates that prepared the electrode terminal in the location which counters are made to intervene between a support substrate and the circuit board and spacing of a chip and the circuit board is extended, a circuit apparatus with the still higher dependability over stress can be obtained.

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[Translation done.]



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## DESCRIPTION OF DRAWINGS

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[Brief Description of the Drawings]

[Drawing 1] Perspective drawing of the support substrate of the semiconductor device in the 1st example of this invention

[Drawing 2] The sectional view of the circuit apparatus which used the support substrate of the semiconductor device in this example

[Drawing 3] The sectional view of the support substrate of the semiconductor device in this example

[Drawing 4] The sectional view of the 2nd support substrate used for other circuit apparatus in this example

[Drawing 5] (a) Perspective drawing of the support substrate of the semiconductor device in the 2nd example of this invention

(b) The sectional view of the circuit apparatus which used the support substrate of the semiconductor device in this example

(c) The sectional view of the support substrate of the semiconductor device in this example

[Drawing 6] The top view of the support substrate of the semiconductor device in the example of others of this invention

[Drawing 7] The production process explanatory view in this example
[Drawing 8] The sectional view of the conventional circuit apparatus
[Drawing 9] (a) The sectional view of the circuit apparatus which used the support substrate of the conventional semiconductor device
(b) The top view of the support substrate of the conventional semiconductor device
(c) The expanded sectional view of this support substrate
[Description of Notations]
2 Electrode for Trial
5 Tape-like Film
11 Semiconductor Device
12 Electrode Terminal
13a Projection electrode
13b Projection electrode
14 Support Substrate
15 Circuit Board
16 Electrode Terminal
19 2nd Support Substrate
21 Electrode Terminal Which Countered Electrode of Semiconductor Device
22 Electrode Terminal Arranged in a Grid Pattern

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[Translation done.]

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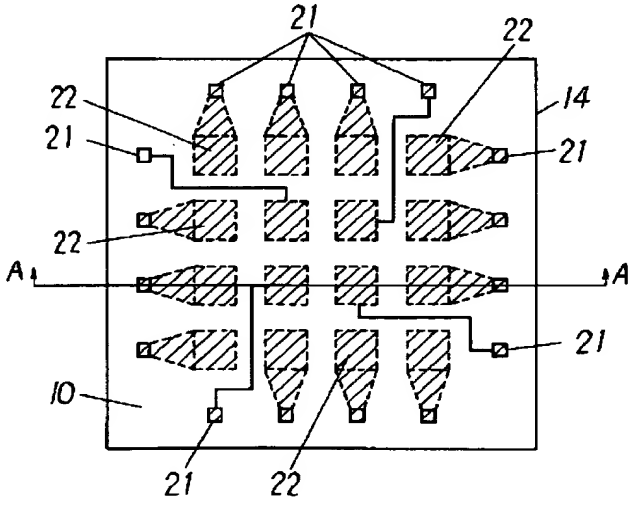
(54)【発明の名称】　半導体素子の支持基板及びそれを使用した回路装置

(57)【要約】

【目的】　半導体素子をフリップチップ実装する際、回路基板と半導体素子との間において突起電極を介して接続する半導体素子の支持基板に関し、従来の突起電極の配列を改善することにより応力の集中による回路装置の不良を低減することを目的とする。

【構成】　支持基板１４の表面には、半導体素子の外周部に沿って設けた電極端子に対向する位置に電極端子２１を設ける。支持基板１４の裏面には表面の電極端子２１と導通する電極端子２２を碁盤目状に配置する。電極端子２１，２２は突起電極にて半導体素子及び回路基板とに接続される。半導体素子と回路基板との熱膨脹係数の差により生じる応力は、碁盤目状に配置された突起電極に分散される。

14　支持基板
21,22　電極端子



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【特許請求の範囲】

【請求項１】　回路基板と外周部に沿って電極端子が設けられた半導体素子との間に配置され、表面には前記半導体素子の電極端子と対向する位置に、突起電極を介して前記半導体素子の電極端子と接続される第１の電極端子を、裏面には前記第１の電極端子と導通し、他の突起電極を介して前記回路基板に設けられた電極端子と接続される第２の電極端子を有する基板であって、少なくとも前記基板の裏面に配置される第２の電極端子の一つが前記第１の電極端子と対向しないように、前記第２の電極端子を前記第１の電極端子よりも内側の位置にも配置したことを特徴とする半導体素子の支持基板。

【請求項２】　第１の電極端子と第２の電極端子とをそれぞれ別の導電体層で形成したことを特徴とする請求項１に記載の半導体素子の支持基板。

【請求項３】　可撓性を有するテープ状の基材上において、第１の電極端子に接続された試験用電極とともに、前記基材の長手方向に連続して形成したことを特徴とする請求項１に記載の半導体素子の支持基板。

【請求項４】　その表面には、外周部に沿って電極端子が設けられた半導体素子の前記電極端子と対向する位置に第１の電極端子が配置され、その裏面には前記第１の電極端子と導通する第２の電極端子が配置され、少なくとも前記第２の電極端子の一つが前記第１の電極端子と対向しないように、前記第２の電極端子を前記第１の電極端子よりも内側の位置にも配置した支持基板を、半導体素子と前記第２の電極端子と対向する位置に電極端子を設けた回路基板との間に介在させ、前記第１の電極端子と前記半導体素子の電極端子との間と、前記第２の電極端子と回路基板の電極端子との間とをそれぞれ突起電極を介して接続してなることを特徴とする半導体素子の支持基板を使用した回路装置。

【請求項５】　その表面には、外周部に沿って電極端子が設けられた半導体素子の前記電極端子と対向する位置に第１の電極端子が配置され、その裏面には前記第１の電極端子と導通する第２の電極端子が配置され、少なくとも前記第２の電極端子の一つが前記第１の電極端子と対向しないように、前記第２の電極端子を前記第１の電極端子よりも内側の位置にも配置した支持基板を、半導体素子と電極端子を設けた回路基板との間に介在させるとともに、前記回路基板と前記支持基板との間に、支持基板の第２の電極端子または前記回路基板の電極端子と対向する位置に電極端子を設けた第２の支持基板を少なくとも１枚以上介在させ、それぞれ対向する電極端子の間を突起電極を介して接続してなることを特徴とする半導体素子の支持基板を使用した回路装置。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は、フリップチップ方式で実装した半導体素子と基板との熱膨脹係数の差によって

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生じる応力を分散し、信頼性を向上させるための半導体素子の支持基板及びそれを使用した回路装置に関する。

【０００２】

【従来の技術】近年、半導体素子を多数個用いる機器の開発が促進されている。半導体実装方法においては機器をより小型化，高機能化するために、より高密度な実装方法の検討が行われており、従来の挿入型であるＤＩＬ型パッケージから面実装型であるＱＦＰ型へ、さらには半導体素子を樹脂モールドしないベアチップ実装方式であるワーヤーボンディング方式やフリップチップ（以下ＦＣ方式と略す）に移行しつつある。

【０００３】以下に従来のＦＣ方式について図８を用いて説明する。図において、１１は半導体素子（以下チップと呼ぶ）、１２はチップ上に形成された電極端子（以下パッドと呼ぶ）、１３は突起電極（以下バンプと呼ぶ）、１５は回路基板であり、１６は回路基板１５上に形成されたパッドである。このようなＦＣ方式は、チップ１１の回路基板１５に対する占有面積がチップ１１のサイズと同等であり、非常に高密度なデバイスを得ることができる。また、チップ１１と回路基板１５間の配線長が他の実装方式に比べ極端に短くなり、渦電流による高周波特性の劣化や信号の遅延も改善される。

【０００４】しかしながら上記の構成では、チップ１１に比べ回路基板１５の熱膨脹係数が大きいために、ヒートサイクル試験で生じた応力により、バンプ１３がパッド１２及び回路基板１５から破断しやすい。この応力に対する信頼性を高めるために、バンプの高さを高くすればヒートサイクル性が向上するという報告もあるが、バンプ材料として半田を用いた場合、バンプ１３を高くするためにはパッド１２のサイズを大きくしなければならず、結果、チップ１１そのものを大きくしなければならず高密度実装からかけ離れた実装形態になる。

【０００５】そこで、図９ａに示すようにチップ１１と回路基板１５との間に樹脂製の支持基板１４を介在させて、それぞれの間をバンプ１３ａ，１３ｂ，１３ｃで接続し、チップ１１の大きさを変えずにヒートサイクル性を向上させようとするものが提案されている（『ＶＬＳＩ　ＣＨＩＰ　ＩＮＴＥＲＣＯＮＮＥＣＴＩＯＮ　ＴＥＣＨＮＯＬＯＧＹ　ＵＳＩＮＧ　ＳＴＡＣＫＥＤ　ＳＯＬＤＥＲ　ＢＵＮＰＳ』　ＩＭＣ　１９９８　Ｐｒｏｃｅｅｄｉｎｇｓ，Ｔｏｋｙｏ，Ｍａｙ２５－２７，１９８８）。この支持基板１４は同図ｂの平面図に示すように、チップ１１のパッド１２と回路基板１５のパッド１６とに対向するように、外周部にパッド１７が形成されている。このパッド１７は同図ｃの支持基板１４の拡大断面図に示すように、支持基板１４の基材となる樹脂製のフィルム３３に形成された透孔３２上に形成され、Ｔｉの金属層３１の両側を銅３０で覆った構造をしている。

【０００６】

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【発明が解決しようとする課題】しかしながら、上記のように支持基板１４を設けるＦＣ方式においても、パッド１７がチップ１１の外周部に設けられた電極端子に対応した位置にのみ形成されているため、ヒートサイクル試験においてチップ１１と回路基板１５の熱膨脹係数の差によって生じる応力が外周部のバンプに集中してしまい、なおも信頼性が劣るという問題を有していた。

【０００７】

【課題を解決するための手段】上記課題を解決するために、本発明の半導体素子の支持基板は、回路基板と外周部に沿って電極端子が設けられた半導体素子との間に配置され、表面には前記半導体素子の電極端子と対向する位置に、突起電極を介して前記半導体素子の電極端子と接続される第１の電極端子を、裏面には前記第１の電極端子と導通し、他の突起電極を介して前記回路基板に設けられた電極端子と接続される第２の電極端子を有する支持基板であって、少なくとも前記基板の裏面に配置される第２の電極端子の一つが前記第１の電極端子と対向しないように、前記第２の電極端子を前記第１の電極端子よりも内側の位置にも配置したものである。

【０００８】

【作用】この構成では、熱膨脹係数の差によってチップや配線基板に生じる応力は、支持基板のチップ占有領域全面に分散して配置したバンプに分散される。このため、外周部にバンプを配置したものに比べて、それぞれのバンプに生じる応力は小さくなり、ヒートサイクル試験においてその信頼性は飛躍的に向上する。

【０００９】

【実施例】以下本発明の実施例について、図面を参照しながら説明する。図１は本発明の第１の実施例における半導体の支持基板の平面図を示すものである。図において、支持基板１４は、基材１０の表面の外周部にチップのパッドに対向するようにバンプが接続されるパッド２１を形成し、基材１０の裏面に回路基板１５とバンプを介して接続するためのパッド２２を碁盤目状に形成してなるものである。図３は図１のＡ－Ａ断面を示すものであり、支持基板１４の内部でパッド２１とパッド２２とは電気的に導通しており、基材１０にそれぞれのパッド２１，２２を形成する導電層２４を形成するための透孔を予め設けておき、そこにラミネート等により支持基板１４を形成するようにしている。

【００１０】また実装方法は、図２に示すようにまずバンプ１３ａの形成されたチップ１１と支持基板１４のパッド２１を接続し、次いで、支持基板１４の裏面の碁盤目状のパッド２２にそれぞれバンプ１３ｂを形成した後に回路基板１５と接続する。なお、さきに述べた実装方法以外にも、予め回路基板上１５にバンプ材料を形成しておき、支持基板１４にチップ１１を接続したモジュールを設置し、加熱によりモジュールと回路基板１５とを接続しても良く、さらには、支持基板１４上にバンプ１３ａ，１３ｂを形成しておき、チップ，支持基板１４，回路基板１５をアライメント後、加熱等の方法にて一括で接続しても良い。

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【００１１】このような支持基板１４を用いれば、バンプ１３ｂを碁盤目状に配置しているために、チップ１１と回路基板１５間に生じる応力を分散させることができ、またチップ１１と回路基板１４との間隔を広げることができるので応力の影響はさらに少なくなる。このように、支持基板と回路基板との間の外周部にのみバンプを形成したものに比べて応力によるバンプの破断等は少なくなり、信頼性の高いＦＣ実装方法が得られる。

【００１２】また、支持基板１４と回路基板１５の間には、図４に示すような支持基板１４のパッド２２と回路基板１５のパッドと対向する位置にパッド３３を形成した第２の支持基板１９を介在させても良く、さらにこの支持基板を多数用いてチップ１１と回路基板１５の間隔を広げ、信頼性をさらに高めることもできる。

【００１３】さて、上記の支持基板１４によると、パッド１３ｂを支持基板１４の裏面全体に配列することにより、パッド２２及びそれらと対向する回路基板１５のパッドを従来のものよりも大きく形成することができる。したがって、実装時の支持基板１４と回路基板１５との位置決めを従来のものより容易にすることができる。

【００１４】図５は本発明の第２の実施例を示すものである。前述の第１の実施例においては、前記導電層２４は一層で形成されているため、パッド２１の真下にはパッド２２を配置することができず、支持基板１４の裏面を必ずしも有効に活用することができない。図５ａに示すようにパッド２１の真下にもパッド２２を配置するためには、そのＢ－Ｂ断面の同図ｃに示すように、支持基板１４内にパッド２１の導電層とパッド２２の導電層とを２層に形成し、上下導電層間を導通させる構成にすれば良い。上下導電層間の接続には、たとえばメッキ法のような既知の方法で行えば良い。

【００１５】以上のように形成された支持基板１４は、パッド２２を大きくしかも各パッド間の間隔も広くすることができるので、同図ｂの回路装置の断面図に示すように、バンプ１３ｂや回路基板１５のパッド１６も大きくしかも間隔をあけて配置できる。このため、回路基板１５と支持基板１４との位置合わせが容易になり、特に、グリーンシート方式を用いるセラミック基板を回路基板とした際に、焼成時のグリーンシート収縮ばらつきによる回路基板１５のパッドの位置がばらつくことを完全にカバーでき、実装時の位置合わせによる歩留まりの低下を極端に抑えることが可能になる。

【００１６】また、本実施例における支持基板１４は、通常のテープキャリア方式での実装に用いられる検査装置及び設備が流用することができ、連続生産性を高めることができる。すなわち、図６に示すように、支持基板１４を可撓性を有するテープ状のフィルム５に連続して

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形成しておけば、図７に示すように、リールトウリールといわれる連続生産が可能になる。図６において、２はパッド２１に導通する試験用電極であり、破線３はチップ１１の外形寸法である。チップ１１の実装時には、送り穴４を設けた一定幅の連続したフィルム５を供給リール６から巻き取りリール７に供給し、ワークエリアWにおいてチップ１１をパッド２１にバンプ１３ａを介して接続した後、試験用電極２によりチップ１１の接続後の試験を行う。この工程の後、良品のみを前記チップ外形３にて打ち抜き、回路基板１５に接続する。

【００１７】このように、支持基板１４と試験用電極２とをテープ状に形成することにより、支持基板１４上にチップ１１を接続した後にモジュールとして試験が可能となり、インラインでの検査が容易に行えるようになる。これにより、回路基板１５への実装歩留まりを飛躍的に向上させることができ、作業性の良い実装方法が得られる。また、試験用電極２は、フィルム５の裏面または両面に形成しても良い。

【００１８】なお、以上の実施例において、パッドは支持基板の裏面に碁盤目状に配置したが、支持基板の裏面全体を有効に利用し、バンプ内に発生する応力を分散させるものであれば他の配列にしても良い。

【００１９】

【発明の効果】以上のように本発明の半導体素子の支持基板は、回路基板とバンプを介して接続するためのパッドを、支持基板の全面に分散して配置したので、回路基板との熱膨脹係数の差により生じる変形及び応力は著しく小さくなる。このため、ヒートサイクルにおける信頼性の高い回路装置を提供することができる。また、これらのパッドの大きさも従来のものに比べて大きく、しかも間隔をあけて形成できるので、回路基板の電極位置のばらつきに影響されることなく、実装時の位置決めを容易に行える。さらに、リールトウリールでの連続生産も可能で、支持基板にチップを載せた状態でチップの動作検査を行うことにより、実装歩留まりを向上させることができる。

【００２０】また、支持基板と回路基板との間に、支持基板の電極端子または回路基板の電極端子と対向する位置に電極端子を設けた第２の支持基板を少なくとも１枚

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以上介在させて、チップと回路基板との間隔を広げるようにすれば、さらに応力に対する信頼性の高い回路装置を得ることができる。

【図面の簡単な説明】

【図１】本発明の第１の実施例における半導体素子の支持基板の透視図

【図２】同実施例における半導体素子の支持基板を使用した回路装置の断面図

【図３】同実施例における半導体素子の支持基板の断面図

【図４】同実施例において他の回路装置に用いられる第２の支持基板の断面図

【図５】（ａ）本発明の第２の実施例における半導体素子の支持基板の透視図

（ｂ）同実施例における半導体素子の支持基板を使用した回路装置の断面図

（ｃ）同実施例における半導体素子の支持基板の断面図

【図６】本発明のその他の実施例における半導体素子の支持基板の平面図

【図７】同実施例における生産工程説明図

【図８】従来の回路装置の断面図

【図９】（ａ）従来の半導体素子の支持基板を使用した回路装置の断面図

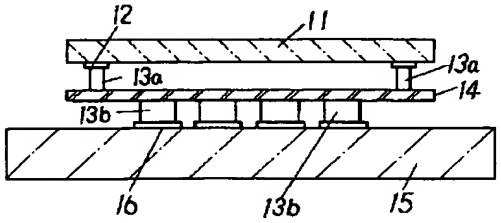
（ｂ）従来の半導体素子の支持基板の平面図

（ｃ）同支持基板の拡大断面図

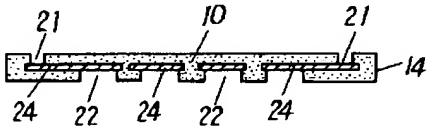
【符号の説明】

２　試験用電極
５　テープ状フィルム
１１　半導体素子
１２　電極端子
１３ａ　突起電極
１３ｂ　突起電極
１４　支持基板
１５　回路基板
１６　電極端子
１９　第２の支持基板
２１　半導体素子の電極に対向した電極端子
２２　碁盤目状に配置した電極端子

【図２】

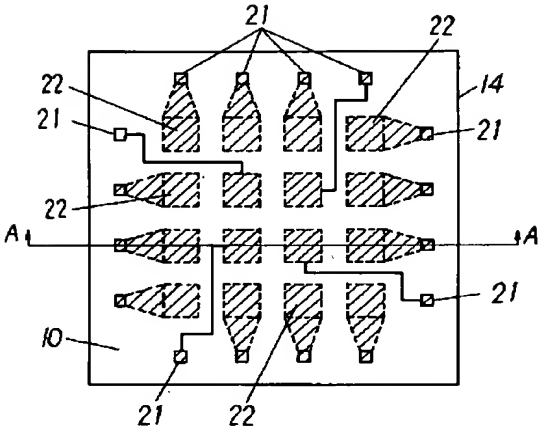



【図３】

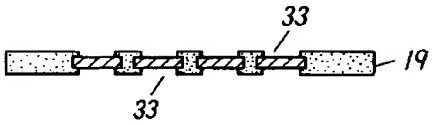


【図１】

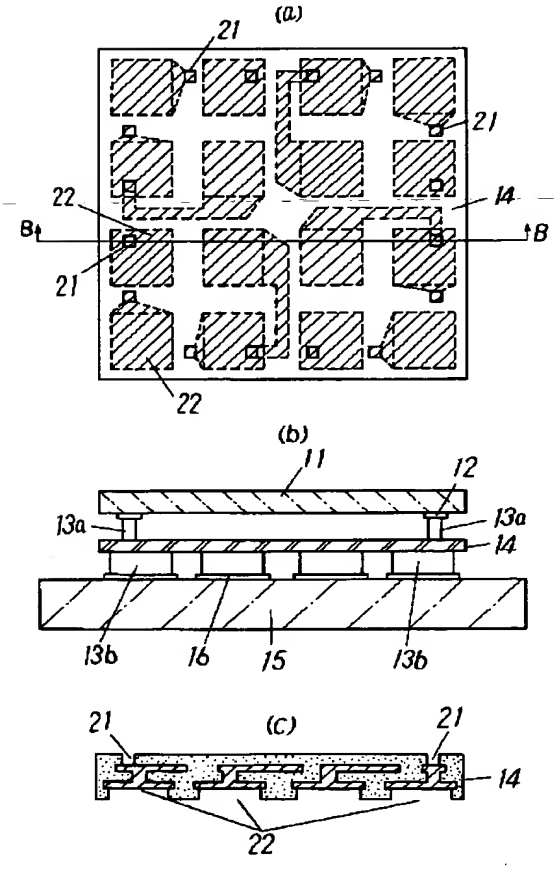
14 支持基板
21,22 電極端子



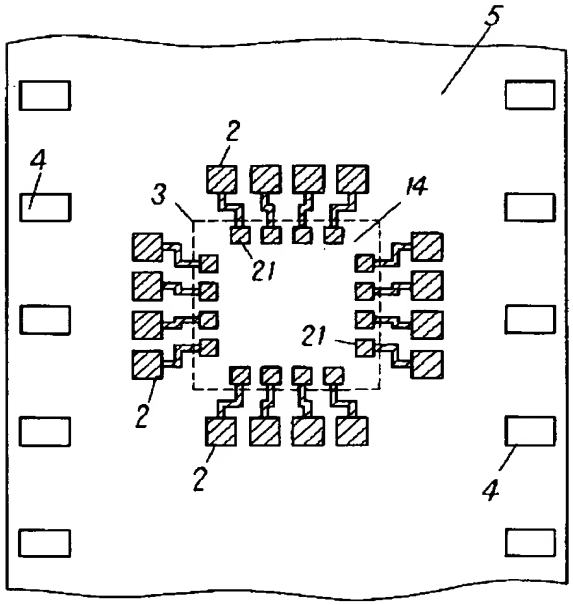

【図４】



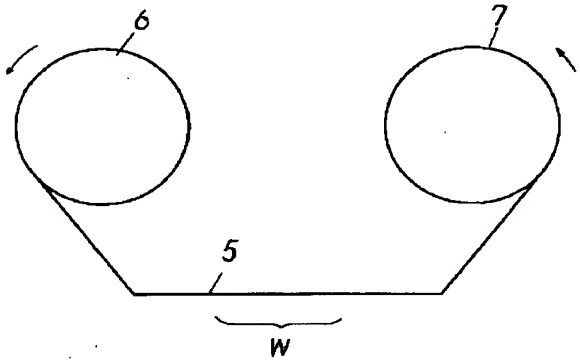

【図５】



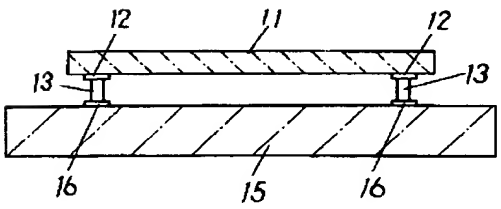

【図６】



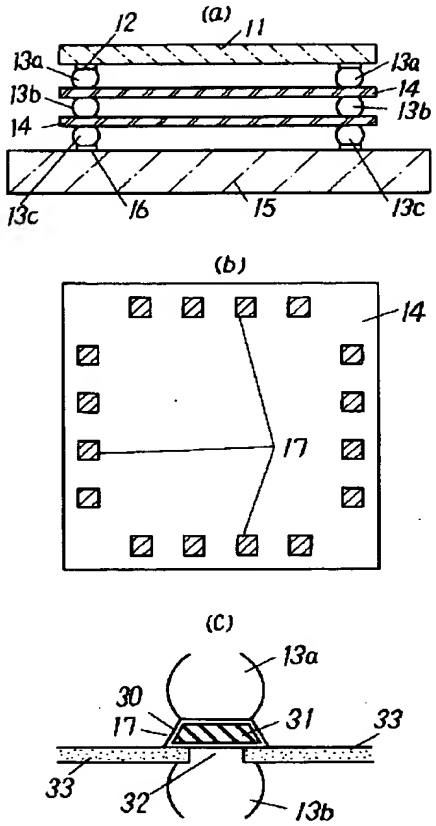

【図７】




【図８】



【図９】


(a)
12
11
13a
13a
13b
14
14
13b
13c
16
15
13c
(b)
14
17
(c)
13a
30
17
31
33
33
32
13b